

What is claimed:

- 1 1. A semiconductor device comprising:
2 an insulation layer;
3 a semiconductor layer formed on the insulation layer;
4 an element isolation region formed in the semiconductor layer; and
5 a first element forming region and a second element forming region defined by the
6 element isolation region;
7 wherein the first element forming region includes both a first bi-polar transistor and a
8 first field effect transistor;
9 the first bi-polar transistor includes a first emitter region of a first conduction type, a
10 first base region of a second conduction type, and a first collector region of the first
11 conduction type,
12 the first field effect transistor includes a first gate electrode layer, a source region of
13 the first conduction type, and a drain region of the first conduction type,
14 the first field effect transistor further includes a first body region of the second
15 conduction type formed at least between the source region of the first conduction type and
16 the drain region of the first conduction type,
17 the first body region of the second conduction type is electrically connected to the
18 source region of the first conduction type,
19 the first body region of the second conduction type is electrically connected to the
20 first base region of the second conduction type,
21 the drain region of the first conduction type is electrically connected to the first
22 collector region of the first conduction type, and
23 the source region of the first conduction type is formed structurally isolated from the
24 first emitter region of the first conduction type, and
25 wherein the second element forming region includes both a second bi-polar transistor
26 and a second field effect transistor,

27 the second bi-polar transistor includes a second emitter region of the first conduction
28 type, a second base region of the second conduction type, and a second collector region of
29 the first conduction type,

30 the second field effect transistor includes a second gate electrode layer, a source
31 region of the second conduction type, and a drain region of the second conduction type,

32 the second field effect transistor further including a first body region of the first
33 conduction type formed at least between the source region of the second conduction type
34 and the drain region of the second conduction type,

35 the first body region of the first conduction type is electrically connected to the
36 second collector region of the first conduction type,

37 the source region of the second conduction type is electrically connected to the
38 second collector region of the first conduction type,

39 the drain region of the second conduction type is electrically connected to the second
40 base region of the second conduction type,

41 the first collector region of the first conduction type is electrically connected to the
42 second emitter region of the first conduction type, and

43 the first gate electrode layer is electrically connected to the second gate electrode
44 layer.

1 2. A semiconductor device according to claim 1, further comprising:

2 a first electrode layer that continues to a side section of the first gate electrode layer
3 and reaches the element isolation region,

4 wherein the first gate electrode layer is formed in a manner to cross over the element
5 forming region,

6 the source region of the first conduction type is formed in a first region surrounded
7 by the first gate electrode layer in a forming region of the first field effect transistor, the first
8 electrode layer, and the element isolation region,

9 the drain region of the first conduction type and the collector region of the first
10 conduction type are formed in a second region surrounded by the first gate electrode layer
11 and the element isolation region,

12 the emitter region of the first conduction type is formed in a third region surrounded
13 by the first gate electrode layer in a forming region of the first bi-polar transistor, the first
14 electrode layer and the element isolation region, and

15 the first body region of the second conduction type is formed at least below the first
16 gate electrode layer in the forming region of the first field effect transistor, and below a part
17 of the first electrode layer.

1 3. A semiconductor device according to claim 2, further comprising:
2 a second electrode layer having one end section that continues to a side section of the
3 second gate electrode layer and another end section that reaches the element isolation
4 region,

5 wherein the second gate electrode layer is formed in a manner to cross over the
6 second element forming region,

7 the drain region of the second conduction type is formed in a fourth region
8 surrounded by the second gate electrode layer in the forming region of the second field
9 effect transistor, the second electrode layer, and the element isolation region,

10 the source region of the second conduction type and the collector region of the first
11 conduction type are formed in a fifth region surrounded by the second gate electrode layer
12 and the element isolation region,

13 the emitter region of the first conduction type is formed in a sixth region surrounded
14 by the second gate electrode layer in the forming region of the second bi-polar transistor, the
15 second electrode layer and the element isolation region, and

16 the first body region of the first conduction type is formed below the second gate
17 electrode layer.

1 4. A semiconductor device according to claim 1, further comprising:
2 a first layer and a second layer, wherein
3 the first layer has one end section continuing to the first gate electrode layer or the
4 second layer, and another end section reaching the element isolation region,
5 the second layer has one end section continuing to the first gate electrode layer or the
6 second layer, and another end section reaching the element isolation region,
7 the source region of the first conduction type is formed in a first region surrounded
8 by the first gate electrode layer, the first layer and the element isolation region,
9 the drain region of the first conduction type and the first collector region of the first
10 conduction type are formed in a second region surrounded by the first gate electrode layer,
11 the second layer and the element isolation region,
12 the first emitter region of the first conduction type is formed in a third region
13 surrounded by the first layer, the second layer and the element isolation region,
14 the first base region of the second conduction type is formed below a part of the first
15 layer, and below a part of the second layer in the semiconductor layer, and
16 the first body region of the second conduction type is formed at least below the first
17 gate electrode layer and below a part of the first layer in the semiconductor layer.

1 5. A semiconductor device according to claim 4, further comprising:
2 a third layer and a fourth layer, wherein
3 the third layer has one end section continuing to the second gate electrode layer or
4 the fourth layer, and another end section reaching the element isolation region,
5 the fourth layer has one end section continuing to the second gate electrode layer or
6 the third layer, and another end section reaching the element isolation region,
7 the drain region of the second conduction type is formed in a fourth region
8 surrounded by the second gate electrode layer, the third layer and the element isolation
9 region,

10 the source region of the second conduction type and the second collector region of
11 the first conduction type are formed in a fifth region surrounded by the second gate electrode
12 layer, the fourth layer and the element isolation region,

13 the second emitter region of the first conduction type is formed in a sixth region
14 surrounded by the third layer, the fourth layer and the element isolation region,

15 the second base region of the second conduction type is formed below a part of the
16 third layer and below a part of the fourth layer in the semiconductor layer, and

17 the first body region of the first conduction type is formed at least below the second
18 gate electrode layer and below a part of the fourth layer in the semiconductor layer, and

19 a second body region of the second conduction type is provided in the semiconductor
20 layer below a part of the third layer for electrically connecting the second body region of the
21 second conduction type and the drain region of the second conduction type.

1 6. A semiconductor device according to claim 1, further comprising, in the first
2 element forming region, a second body region of the first conduction type, which is formed
3 in the semiconductor layer between the first base region of the second conduction type and
4 the first collector region of the first conduction type.

1 7. A semiconductor device according to claim 1, wherein an impurity diffusion
2 layer of the second conduction type is further formed in the first element forming region,

3 wherein the impurity diffusion layer of the second conduction type is a
4 semiconductor layer in the first region, and is formed in the semiconductor layer between
5 the source region of the first conduction type and the first body region of the second
6 conduction type, and

7 the source region of the first conduction type and the first body region of the second
8 conduction type are electrically connected to one another through the impurity diffusion
9 layer of the second conduction type.

1 8. A semiconductor device according to claim 7, wherein a contact layer for
2 electrically connecting the impurity diffusion layer of the second conduction type and the
3 source region of the first conduction type is formed, wherein the contact layer is formed in a
4 manner to cross over the impurity diffusion layer of the second conduction type and the
5 source region of the first conduction type.

1 9. A semiconductor device according to claim 1, wherein a third body region of
2 the second conduction type is formed in the semiconductor layer between the first collector
3 region of the first conduction type and the first emitter region of the first conduction type
4 and in the semiconductor layer adjacent to the element isolation region.

1 10. A semiconductor device according to any one of claim 8, wherein a contact
2 layer for electrically connecting the source region of the second conduction type and the
3 second contact region of the first conduction type is formed in the second element isolation
4 region, wherein the contact layer is formed in a manner to cross over the source region of
5 the second conduction type and the second collector region of the first conduction type.

1 11. A semiconductor device according to any one of claim 9, wherein a fourth
2 body region of the second conduction type is formed in the semiconductor layer between the
3 second collector region of the first conduction type and the second emitter region of the first
4 conduction type, and in the semiconductor layer adjacent to the element isolation region.

1 12. A semiconductor device according to claim 1, wherein the first conduction
2 type is n-type, and the second conduction type is p-type.

1 13. A semiconductor device according to claim 1, wherein the first conduction
2 type is p-type, and the second conduction type is n-type.

14. A semiconductor device according to claim 1, wherein the semiconductor layer is a silicon layer.

15. A semiconductor device comprising:
an insulation layer;
a semiconductor layer formed on the insulation layer;
an element isolation region formed in the semiconductor layer; and
a first element forming region and a second element forming region defined by the element isolation region,
wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor,
a first gate electrode layer is formed on the semiconductor layer,
the first gate electrode layer is formed in a manner to cross over the first element forming region,
a first electrode layer is formed on the semiconductor layer,
the first electrode layer has one end section continuing to a side section of the first gate electrode layer, and another end section reaching the element isolation region,
a first impurity diffusion layer of a first conduction type is formed at least in a part of a first region surrounded by the first gate electrode layer in a forming region of the first field effect transistor, the first electrode layer and the element isolation region,
a second impurity diffusion layer of the first conduction type is formed in a second region surrounded by the first gate electrode layer and the element isolation region,
a third impurity diffusion layer of the first conduction type is formed in a third region defined by the first gate electrode layer in a forming region of the first bi-polar transistor, the first electrode layer and the element isolation region,
a first body region of a second conduction type is formed below the first gate electrode layer in a forming region of the first field effect transistor and the first electrode layer,

26 a first impurity diffusion layer of the second conduction type is formed below the
27 first gate electrode layer in the forming region of the first bi-polar transistor and the first
28 electrode layer and along a periphery of the third impurity diffusion layer of the first
29 conduction type,
30 the first body region of the second conduction type is electrically connected to the
31 first impurity diffusion layer of the first conduction type, and
32 the first body region of the second conduction type is electrically connected to the
33 first impurity diffusion layer of the second conduction type,
34 wherein the second element forming region includes both a second bi-polar transistor
35 and a second field effect transistor,
36 a second gate electrode layer is formed on the semiconductor layer,
37 the second gate electrode layer is formed in a manner to cross over the second
38 element forming region,
39 a second electrode layer is formed on the semiconductor layer,
40 the second electrode layer has one end section continuing to a side section of the
41 second gate electrode layer, and another end section reaching the element isolation region,
42 a second impurity diffusion layer of the second conduction type is formed in a fourth
43 region surrounded by the second gate electrode layer in a forming region of the second field
44 effect transistor, the first electrode layer and the element isolation region,
45 a third impurity diffusion layer of the second conduction type is formed in a fifth
46 region surrounded by the second gate electrode layer and the element isolation region and in
47 the forming region of the second field effect transistor,
48 a fourth impurity diffusion layer of the first conduction type is formed in a fifth
49 region in a forming region of the second bi-polar transistor,
50 a fifth impurity diffusion layer of the first conduction type is formed in a sixth region
51 surrounded by the second gate electrode layer in the forming region of the second bi-polar
52 transistor and the element isolation region,
53 a body region of the first conduction type is formed below the second gate electrode
54 layer,

55 a fourth impurity diffusion layer of the second conduction type is formed below the
 56 second gate electrode layer in the forming region of the second bi-polar transistor and the
 57 second electrode layer and along a periphery of the fifth impurity diffusion layer of the first
 58 conduction type,

59 the body region of the first conduction type is electrically connected to the fourth
 60 impurity diffusion layer of the first conduction type,

61 the third impurity diffusion layer of the second conduction type is electrically
 62 connected to the fourth impurity diffusion layer of the first conduction type,

63 the second impurity diffusion layer of the second conduction type is electrically
 64 connected to the fourth impurity diffusion layer of the second conduction type,

65 the second impurity diffusion layer of the first conduction type is electrically
 66 connected to the fifth impurity diffusion layer of the first conduction type, and

67 the first gate electrode layer is electrically connected to the second gate electrode
 68 layer.

1 (16.) A method for manufacturing a semiconductor device including an insulation
 2 layer and a semiconductor layer formed on the insulation layer, the method comprising the
 3 steps of:

4 (A) forming an element isolation region in the semiconductor layer to define a first
 5 element forming region and a second element forming region; and

6 (B) forming a first field effect transistor and a first bi-polar transistor in the first
 7 element forming region,

8 wherein the step (B) comprises the steps of:

9 (B - 1) forming a first body region of a second conduction type in the semiconductor
 10 layer at least in a forming region where a first gate electrode layer is to be formed,

11 (B - 2) forming a first gate electrode layer and a first electrode layer on the
 12 semiconductor layer in the first element forming region, wherein the first electrode layer
 13 continues to the first gate electrode layer and reaches the element isolation region,

(B - 3) forming a first impurity diffusion layer of the second conduction type in the semiconductor layer in a third region surrounded by the first gate electrode layer in a forming region of the bi-polar transistor, the first electrode layer and the element isolation region,

(B - 4) conducting a thermal treatment to thermally diffuse the first impurity diffusion layer of the second conduction type to form a first base region of the second conduction type of the first bi-polar transistor below a part of the first gate electrode layer and in the semiconductor layer below the first electrode layer, and to electrically connect the first base region of the second conduction type and the first body region of the second conduction type,

(B - 5) forming a source region of a first conduction type of the first field effect transistor at least in a part of a first region surrounded by a first gate electrode layer in a forming region of the first field effect transistor, the first electrode layer and the element isolation region,

(B - 6) forming a drain region of the first conduction type of the first field effect transistor in a part of a second region surrounded by the first gate electrode layer and the element isolation region,

(B - 7) forming a first collector region of the first conduction type of the first bi-polar transistor in a part of the second region,

(B - 8) forming a first emitter region of the first conduction type of the first bi-polar transistor in the third region, and

(B - 9) electrically connecting the first body region of the second conduction type and the source region of the first conduction type;

the step (C) of forming a second field effect transistor and a second bi-polar transistor in the second element forming region,

wherein the step (C) comprises the steps of:

(C - 1) forming a first body region of the first conduction type in the semiconductor layer at least in a forming region where a second gate electrode layer is to be formed,

42 (C - 2) forming a second body region of the second conduction type at least in a part
43 of the semiconductor layer in a forming region where a second electrode layer is to be
44 formed,

45 (C - 3) forming a second gate electrode layer and a second electrode layer on the
46 semiconductor layer in the second element forming region, wherein the second electrode
47 layer has one end section continuing to a side section of the gate electrode layer and another
48 end section reaching the element isolation region,

49 (C - 4) forming a second impurity diffusion layer of the second conduction type in
50 the semiconductor layer in a sixth region surrounded by the second gate electrode layer in a
51 forming region of the second bi-polar transistor, the second electrode layer and the element
52 isolation region,

53 (C - 5) conducting a thermal treatment to thermally diffuse the second impurity
54 diffusion layer of the second conduction type to form a second base region of the second
55 conduction type of the second bi-polar transistor below a part of the second gate electrode
56 layer and in the semiconductor layer below the second electrode layer, and to electrically
57 connect the second base region of the second conduction type and the second body region of
58 the second conduction type,

59 (C - 6) forming a drain region of the second conduction type of the second field
60 effect transistor in a fourth region surrounded by a second gate electrode layer in a forming
61 region of the second field effect transistor, the second electrode layer and the element
62 isolation region, and electrically connecting the drain region of the second conduction type
63 to the second base region of the second conduction type through the second body region of
64 the second conduction type,

65 (C - 7) forming a source region of the second conduction type of the second field
66 effect transistor in a part of a fifth region surrounded by the second gate electrode layer and
67 the element isolation region,

68 (C - 8) forming a second collector region of the first conduction type of the second
69 bi-polar transistor in a part of the fifth region, and electrically connecting the second

70 collector region of the first conduction type to the first body region of the first conduction
71 type,

72 (C - 9) forming a second emitter region of the first conduction type of the second bi-
73 polar transistor in the sixth region, and

74 (C - 10) electrically connecting the source region of the second conduction type and
75 the second collector region of the first conduction type;

76 the step (D) of electrically connecting the first collector region of the first conduction
77 type and the second emitter region of the first conduction type; and

78 the step (E) of electrically connecting the first gate electrode layer and the second
79 gate electrode layer.

1 (17) A method for manufacturing a semiconductor device including an insulation
2 layer and a semiconductor layer formed on the insulation layer, the method comprising the
3 steps of:

4 (A) forming an element isolation region in the semiconductor layer to define a first
5 element forming region and a second element forming region; and

6 (B) forming a first field effect transistor and a first bi-polar transistor in the first
7 element forming region,

8 wherein the step (B) comprises the steps of:

9 (B - 1) forming a first body region of a second conduction type in the semiconductor
10 layer at least in a forming region where a first gate electrode layer is to be formed and in a
11 forming region where a first layer is to be formed,

12 (B - 2) forming a first gate electrode layer on the semiconductor layer in the first
13 element forming region,

14 (B - 3) forming a first layer on the semiconductor layer in the first element forming
15 region, the first layer having one end section continuing to the first gate electrode layer or a
16 second layer, and another end section reaching the element isolation region,

17 (B - 4) forming a second layer on the semiconductor layer in the first element
18 forming region, the second layer having one end section continuing to the first gate electrode
19 layer or the first layer, and another end section reaching the element isolation region,
20 (B - 5) forming a first impurity diffusion layer of the second conduction type in the
21 semiconductor layer in a third region surrounded by the first layer, the second layer and the
22 element isolation region,
23 (B - 6) conducting a thermal treatment to thermally diffuse the first impurity
24 diffusion layer of the second conduction type to form a first base region of the second
25 conduction type of the first bi-polar transistor below a part of the first layer and in the
26 semiconductor layer below a part of the second layer, and to electrically connect the first
27 base region of the second conduction type and the first body region of the second conduction
28 type,
29 (B - 7) forming a source region of a first conduction type of the first field effect
30 transistor at least in a part of a first region surrounded by the gate electrode layer, the first
31 layer and the element isolation region,
32 (B - 8) forming a drain region of the first conduction type of the first field effect
33 transistor in a part of a second region surrounded by the gate electrode layer, the second
34 layer and the element isolation region,
35 (B - 9) forming a first collector region of the first conduction type of the first bi-
36 polar transistor in a part of a second region surrounded by the first gate electrode layer, the
37 second layer and the element isolation region,
38 (B - 10) forming a first emitter region of the first conduction type of the first bi-polar
39 transistor in a third region surrounded by the first layer, the second layer and the element
40 isolation region, and
41 (B - 11) electrically connecting the first body region of the second conduction type
42 and the source region of the first conduction type;
43 the step (C) of forming a second field effect transistor and a second bi-polar
44 transistor in the second element forming region,
45 wherein the step (C) comprises the steps of:

46 (C - 1) forming a first body region of the first conduction type in the semiconductor
47 layer at least in a forming region where a second gate electrode layer is to be formed and a
48 forming region where a fourth layer is to be formed,

49 (C - 2) forming a second body region of the second conduction type at least in a part
50 of the semiconductor layer in a forming region where a third layer is to be formed,

51 (C - 3) forming a second gate electrode layer on the semiconductor layer in the
52 second element forming region,

53 (C - 4) forming a third layer on the semiconductor layer in the second element
54 forming region, wherein the third layer has one end section continuing to the second gate
55 electrode layer or the fourth layer, and another end section reaching the element isolation
56 region,

57 (C - 5) forming a fourth layer on the semiconductor layer in the second element
58 forming region, wherein the fourth layer has one end section continuing to the second gate
59 electrode layer or the third layer, and another end section reaching the element isolation
60 region,

61 (C - 6) forming a second impurity diffusion layer of the second conduction type in
62 the semiconductor layer in a sixth region surrounded by the third layer, the fourth layer and
63 the element isolation region,

64 (C - 7) conducting a thermal treatment to thermally diffuse the second impurity
65 diffusion layer of the second conduction type to form a second base region of the second
66 conduction type of the second bi-polar transistor below a part of the third layer and in the
67 semiconductor layer below a part of the fourth layer, and to electrically connect the second
68 base region of the second conduction type and the second body region of the second
69 conduction type,

70 (C - 8) forming a drain region of the second conduction type of the second field
71 effect transistor in a fourth region surrounded by the second gate electrode layer, the third
72 layer and the element isolation region,

73 and electrically connecting the drain region of the second conduction type to the
74 second base region of the second conduction type through the second body region of the
75 second conduction type,
76 (C – 9) forming a source region of the second conduction type of the second field
77 effect transistor in a part of a fifth region surrounded by the second gate electrode layer, the
78 fourth layer and the element isolation region,
79 (C – 10) forming a second collector region of the first conduction type of the second
80 bi-polar transistor in a part of a fifth region surrounded by the second gate electrode layer,
81 the fourth layer and the element isolation region,
82 and electrically connecting the second collector region of the first conduction type to
83 the first body region of the first conduction type,
84 (C – 11) forming a second emitter region of the first conduction type of the second
85 bi-polar transistor in a sixth region surrounded by the third layer, the fourth layer and the
86 element isolation region, and
87 (C – 12) electrically connecting the source region of the second conduction type and
88 the second collector region of the first conduction type;
89 the step (D) of electrically connecting the first collector region of the first conduction
90 type and the second emitter region of the first conduction type; and
91 the step (E) of electrically connecting the first gate electrode layer and the second
92 gate electrode layer.

1 18. A method for manufacturing a semiconductor device according to claim 17,
2 further comprising the step of forming a third body region of the second conduction type in
3 the semiconductor layer below the second layer in the first element forming region and in
4 the semiconductor layer adjacent to the element isolation region.

1 19. A method for manufacturing a semiconductor device according to claim 18,
2 further comprising the step of forming a fourth body region of the second conduction type in
3 the semiconductor layer below the fourth layer in the second element forming region and in
4 the semiconductor layer adjacent to the element isolation region.

1 20. A method for manufacturing a semiconductor device according to claim 17,
2 wherein the first conduction type is n-type, and the second conduction type is p-type.

1 21. A method for manufacturing a semiconductor device according to claim 17,
2 wherein the first conduction type is p-type, and the second conduction type is n-type.

1 22. A method for manufacturing a semiconductor device according to claim 17,
2 wherein the semiconductor layer is a silicon layer.